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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1 52(b))

Attorney Docket No	AMKOR-017A
First Inventor	Jong Sik Paek
Title	SEMICONDUCTOR PACKAGE WITH STACKED DIES
Express Mail Label No	EV 015373454 US

APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. [X] Fee Transmittal Form (e g , PTO/SB17)
2. [ ] Applicant claims small entity status
3. [X] Specification [Total Pages 16]
(preferred arrangement set forth below)
-Descriptive title of the invention
-Cross Reference to Related Applications
-Statement Regarding Fed sponsored R &
-Reference to sequence listing, a table, or
a computer program listing appendix
-Background of the Invention
-Brief Summary of the Invention
-Brief Description of the Drawings (if filed)37 CFR 3 73(b)
-Detailed Description
-Claim(s)
-Abstract of the DisclosureCopies of IDS Citations
4. [X] Drawing(s) (35 U S C 113) [Total Sheets 4]
5. [X] Oath or Declaration [Total Pages 2]
a [X] Newly executed (original or copy)
b [ ] Copy from a prior application (37 CFR 1 63(d))
(for continuation/divisional with Box 17 completed)
i [ ] DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1 63(d)(2) and 1 33(b)
6. [ ] Application Data Sheet. See 37 CFR 1 76

7 [ ] CD-ROM or C-R in duplicate, large table or Computer Program (Appendix)
8 [ ] Nucleotide and/or Amino Acid Sequence Submission
See 37 CFR 1 27 (if applicable, all necessary)
a [ ] Computer Readable Form (CRF)
b [ ] Specification Sequence Listing on:
i [ ] CD-ROM or CD-R (2 copies), or
ii [ ] paper
c [ ] Statements verifying identity of above copies
a computer program listing appendix

ACCOMPANYING APPLICATION PARTS

9 [X] Assignment Papers (cover sheet & document(s))
10 [ ] 37 CFR 3 73(b) Statement [ ] Power of Attorney
11 [ ] English Translation Document (if applicable)
12 [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
13 [ ] Preliminary Amendment
14 [X] Return Receipt Postcard (MPEP 503) (Should be specifically
15 [X] Certified Copy of Priority Document(s)
(if foreign priority is claimed)
16 [ ] Other _____

17. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in a preliminary amendment, or in an Application Data Sheet under 37 CFR 1 76:

[ ] Continuation [ ] Divisional [ ] Continuation-in-part of prior application No _____

Prior application information Examiner _____ Group/Art Unit _____

For CONTINUATION OR DIVISIONAL APPS only The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 5b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts

18. CORRESPONDENCE ADDRESS

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Name (Print/Type)	Mark B Garred	Registration No (Attorney/Agent)	34,823
Signature		Date	1/11/02

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FEE TRANSMITTAL for FY 2002

Patent fees are subject to annual revision.

TOTAL AMOUNT OF PAYMENT	($)740 00

Complete if Known	
Application Number	Unknown
Filing Date	Herewith
First Named Inventor	Jong Sik Paek
Examiner Name	Unknown
Group Art Unit	Unknown
Attorney Docket No	AMKOR-017A

METHOD OF PAYMENT

1. ☐ The Commissioner is hereby authorized to charge indicated fees and credit any overpayments to.

Deposit Account Number: 19-4330

Deposit Account Name: Stetina Brunda

X Charge Any Additional Fee Required Under 37 CFR 1 16 and 1 17
☐ Applicant claims small entity status See 37 CFR 1 27

2. ☒ **Payment Enclosed:**

X Check ☐ Credit card ☐ Money Order ☐ Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	740	201	370	Utility Filing fee	$740 00
106	330	206	165	Design Filing fee	
107	510	207	255	Plant Filing fee	
108	740	208	370	Reissue Filing fee	
114	160	214	805	Provisional Filing fee	

SUBTOTAL (1) $740 00

2. EXTRA CLAIM FEES

	Extra Claims	Fee from below	Fee Paid
Total Claims ____ - 20** =	____	X ____ =	
Independent Claims ____ - 3 =	____	X ____ =	
Multiple Dependent		=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	84	202	42	Independent claims in excess of 3
104	280	204	140	
109	80	209	40	
110	18	210	9	

SUBTOTAL (2) $ ____

**or number previously paid, if greater, For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge -late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for ex parte reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	400	216	200	Extension for reply within second month	
117	920	217	460	Extension for reply within third month	
118	1,440	218	720	Extension for reply within fourth month	
128	1,960	228	980	Extension for reply within fifty month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a brief in support of an appeal	
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive-unavoidable	
141	1,240	241	620	Petition to revive-unintentional	
142	1,240	242	620	Utility issue fee (or reissue)	
143	440	243	220	Design issue fee	
144	600	244	300	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	180	126	180	Submission of Information Disclosure Statement	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	710	246	355	Filing a submission after final rejection (37 CFR § 1 129(a))	
149	710	249	355	For each additional invention to be examined	
179	710	279	355	Request for Continued Examination (RCE)	
169	900	169	900	Request for expedited examination of a design application	

Other fee (specify) ____

* Reduced by Basic Filing Fee Paid SUBTOTAL (3) $ ____

SUBMITTED BY: Complete (if applicable)

Name (Print/Type)	Mark B Garred	Registration No (Attorney/Agent)	34,823	Telephone	(949) 855-1246
Signature				Date	1/11/02

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ATTORNEY DOCKET: AMKOR-017A

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on January 11, 2002 .
(Date)

Kristin Stenberg
Signature

Kristin Stenberg
Typed or printed name of person signing Certificate

Note: Each paper must have its own certificate of mailing, or this certificate must identify each submitted paper.

1. Utility Patent Application Transmittal;
2. Fee Transmittal (in duplicate);
3. Specification (16 pages);
4. Drawings (4 pages);
5. Declaration (2 pages);
6. Recordation Form Cover Sheet;
7. Assignment;
8. Check for $40.00 (Assignment Fee);
9. Certified Copy of Priority Document;
10. Check for $740.00; and
11. Return Receipt Postcard

Case No.: AMKOR-017A (SK-017A)

SEMICONDUCTOR PACKAGE WITH STACKED DIES

INVENTOR
Jong Sik Paek

CROSS-REFERENCE TO RELATED APPLICATIONS

The present application claims priority to Korean Patent Application No. 2001-02163 entitled SEMICONDUCTOR PACKAGE filed January 15, 2001.

STATEMENT RE: FEDERALLY SPONSORED RESEARCH/DEVELOPMENT
(Not Applicable)

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates generally to semiconductor packages, and more particularly to a semiconductor package which includes a stacked pair of semiconductor dies, one of which is electrically connected to the leads of the semiconductor package in a manner facilitating a reduction in the size of the semiconductor package.

2. Description of the Related Art

[0002] As is well known in the electrical arts, recent advances in semiconductor package technology have led to the development of packaging techniques which provide for the continuing miniaturization of the semiconductor package. These advancements have also led to the

development of a wide variety of new and differing types of semiconductor packages. Consistently in high demand are those semiconductor packages which have a high capacity and are capable of performing various functions. However, those currently known semiconductor packages including only a single semiconductor die are limited in their ability to perform multi-functions. To address this limitation, there has been developed in the prior art various semiconductor packages in which semiconductor dies or the semiconductor packages themselves are stacked on each other. However, these semiconductor packages have structural limits attributable to the stacking of the dies or packages therein, and are often of a size which decreases or diminishes their utility in certain applications. The present invention is specifically adapted to address this deficiency, as will be discussed in more detail below.

BRIEF SUMMARY OF THE INVENTION

[0003] In accordance with the present invention, there is provided a semiconductor package which comprises a plurality of leads. Each of the leads defines opposed first and second surfaces, and a third surface which is also disposed in opposed relation to the second surface. The first surface is oriented between the second and third surfaces. Also included in the semiconductor package are first and second semiconductor dies which each define opposed first and second surfaces. A plurality of bond pads are disposed on the first surface of the first semiconductor die, with bond pads also being disposed on the second surface of the second semiconductor die. The first surface of the first semiconductor die is attached to the second surface of each of the leads, with the first surface of the second semiconductor die being attached to

the second surface of the first semiconductor die.

[0004] In the semiconductor package, a plurality of conductive wires are used to electrically connect the bond pads of the first semiconductor die to respective ones of the first surfaces of the leads. Conductive wires are also used to electrically connect the bond pads of the second semiconductor die to respective ones of the second surfaces of the leads. An encapsulating portion is applied to the leads, the first and second semiconductor dies, and the conductive wires, with the third surface of each of the leads being exposed within the encapsulating portion.

[0005] In the semiconductor package of the present invention, the first semiconductor die and the leads are oriented relative to each other such that each of the bond pads of the first semiconductor die is located between a respective pair of the leads. As such, the bond pads of the first semiconductor die do not contact the second surface of any one of the leads. The conductive wires electrically connecting the bond pads of the first semiconductor die to the leads are thus oriented inwardly relative to the peripheral edge of the first semiconductor die. This relative orientation facilitates a reduction in the size of the semiconductor package.

[0006] The present invention is best understood by reference to the following detailed description when read in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] These, as well as other features of the present invention, will become more apparent upon reference to the drawings wherein:

[0008] Figure 1 is a cross-sectional view of a semiconductor package constructed in accordance with the

present invention;

[0009] Figure 1A is a bottom plan view of the semiconductor package shown in Figure 1, excluding the encapsulating portion thereof;

[0010] Figure 1B is a top plan view of the semiconductor package shown in Figure 1, excluding the encapsulating portion thereof; and

[0011] Figures 2A through 2E are cross-sectional views illustrating a sequence of steps which may be employed for manufacturing the semiconductor package of the present invention.

[0012] Common reference numerals are used throughout the drawings and detailed description to indicate like elements.

DETAILED DESCRIPTION OF THE INVENTION

[0013] Referring now to the drawings wherein the showings are for purposes of illustrating a preferred embodiment of the present invention only, and not for purposes of limiting the same, Figure 1 provides a cross-sectional view of a semiconductor package 100 constructed in accordance with the present invention. The semiconductor package 100 comprises a plurality of identically configured leads 130. Each of the leads 130 defines a generally planar first (lower) surface 131a and a generally planar second (upper) surface 131b which is disposed in opposed relation to the first surface 131a. Each lead 130 further defines a generally planar third (lower) surface 131c which is also disposed in opposed relation to the second surface 131b and is laterally offset outwardly relative to the first surface 131a. More particularly, the thickness between the second and third surfaces 131b, 131c exceeds the thickness between the first and second surfaces 131a, 131b. The first surfaces 131a of

the leads 130 are each preferably formed by a conventional half etching technique using chemical solutions.

[0014] In addition to the leads 130, the semiconductor package 100 includes a die paddle 135 which is of a predetermined thickness. The preferred thickness of the die paddle 135 is preferably the same as the thickness between the second and third surfaces 131b, 131c of each of the leads 130. The leads 130 and die paddle 135 are oriented relative to each other such that the leads 130 are arranged about the periphery of the die paddle 135 in the manner best shown in Figure 1A. The die paddle 135 has a generally square configuration, with the leads 130 being segregated into four sets of four, and each set extending along a respective one of the four peripheral edge segments defined by the die paddle 135. As seen in Figures 1 and 1A, the innermost end of each lead 130 is disposed in spaced relation to the corresponding peripheral edge segment of the die paddle 135. Those of ordinary skill in the art will recognize that differing numbers of leads 130 in differing arrangements may be included in the semiconductor package 100, with the size, shape and arrangement of the leads 130 and die paddle 135 as shown in Figures 1, 1A and 1B being for exemplary purposes only.

[0015] The semiconductor package 100 of the present invention further comprises a first semiconductor die 110 which defines a first surface 111a and a second surface 111b which is disposed in opposed relation to the first surface 111a. The first semiconductor die 110 further includes a plurality of bond pads 113 which are disposed on the first surface 111a thereof. In the semiconductor package 100, portions of the first surface 111a of the first semiconductor die 110 are bonded to the second surface 131b of each lead 130 and to the top surface of the die paddle 135 through the use of a layer of a die attach

material 160. The die attach material 160 may be any one of a non-conductive epoxy, a non-conductive polyimide, a non-conductive double-faced adhesive tape or its equivalent, with the present invention not being limited by any particular die attach material 160.

[0016] In addition to the first semiconductor die 110, the semiconductor package 100 includes a second semiconductor die 120. The second semiconductor die 120 defines a first surface 121a and a second surface 121b which is disposed in opposed relation to the first surface 121a. Disposed on the second surface 121b are a plurality of bond pads 123. The first surface 121a of the second semiconductor die 120 is bonded to the second surface 111b of the first semiconductor die 110 by another layer of the die attach material 160.

[0017] As seen in Figure 1A, the first semiconductor die 110 and leads 130 are arranged relative to each other such that the bond pads 113 of the first semiconductor die 110 are each oriented between a respective pair of the leads 130 when the first surface 111a of the first semiconductor die 110 is bonded to the second surfaces 131b of the leads 130. In this regard, it is important in the semiconductor package 100 that none of the bond pads 113 contact any of the second surfaces 131b of the leads 130 when the first surface 111a of the semiconductor die 110 is bonded to the second surfaces 131b of the leads 130. In the semiconductor package 100, each bond pad 113 of the first semiconductor die 120 is electrically connected to the first surface 131a of a respective one of the leads 130 by a first conductive connector 151 such as a conductive wire. Similarly, as seen in Figures 1 and 1B, each bond pad 123 of the second semiconductor die 120 is electrically connected to the second surface 131b of a respective one of the leads 130 by a second conductive connector 153 such as

a conductive wire. The conductive connectors 151, 153 may each be any one of a gold wire, an aluminum wire, or its equivalent, with the present invention not being limited by any particular material for the conductive connectors 151, 153.

[0018] As indicated above, the bond pads 113 of the first semiconductor die 110 are each located between a respective pair of leads 130. Thus, the electrical connection between the bond pads 113 and the first surfaces 131a of the leads 130 through the use of the conductive connectors 151 can be accomplished in a manner wherein the conductive connectors 151 are each located inwardly relative to the peripheral edge of the first semiconductor die 110. As seen in Figure 1, the peripheral edge of the first semiconductor die 110 extends to approximately that portion of the second surface 131b of each lead 130 which is disposed in opposed relation to the third surface 131c.

[0019] In the semiconductor package 100, the first and second semiconductor dies 110, 120, the leads 130, and the conductive connectors 151, 153 are each encapsulated by an encapsulant in order to protect the same from the external environment. The hardening of the encapsulant defines an encapsulating portion 180 of the semiconductor package 100. The encapsulating portion 180 is formed such that the third surface 131c of each of the leads 130 and the bottom surface of the die paddle 135 are exposed within the encapsulating portion 180, and in particular the bottom surface defined thereby. Also exposed in the side surfaces of the encapsulating portion 180 is the outermost end of each of the leads 130. The exposed third surfaces 131c of the leads 130 may be electrically connected to an external device (e.g., a motherboard). Additionally, the exposed third surfaces 131c of the leads 130 and bottom surface of the die paddle 135 within the encapsulating portion 180

function as heat sinks which allow for the emission of heat generated by the first and second semiconductor dies 110, 120.

[0020] It is contemplated that the first and second semiconductor dies 110, 120 will have identical functions since the semiconductor dies 110, 120 are electrically connected to common leads 130. However, it is also contemplated that the first and second semiconductor dies 110, 120 may have different functions. In this case, the first semiconductor die 110 would be electrically connected to the first surfaces 131a of certain ones of the leads 130, with the second semiconductor die 120 being electrically connected to the second surfaces 131b of certain ones of the leads 130 which are not electrically connected to the first semiconductor die 110. As such, the first and second semiconductor dies 110, 120 would not be electrically connected to any common lead 130. The orientation of the conductive connectors 151 inwardly of the peripheral edges of the stacked semiconductor dies 110, 120 allows for a reduction in the size of the semiconductor package 100.

[0021] Referring now to Figures 2A through 2E, the manufacturing method for the semiconductor package 100 of the present invention preferably comprises the initial step of providing the leads 130 and die paddle 135 oriented relative to each other in the above-described manner. Thereafter, the first surface 111a of the first semiconductor die 110 is bonded to the second surface 131b of each of the leads 130 and to the top surface of the die paddle 135 through the use of the die attach material 160 in the above-described manner (Figure 2A). As explained above, the first semiconductor die 110 and the leads 130 are oriented relative to each other such that the bond pads 113 of the first semiconductor die 110 are not in direct

contact with any of the second surfaces 131b of the leads 130, but rather are each oriented between a respective pair of the leads 130.

[0022] Subsequent to the attachment of the first semiconductor die 110 to the leads 130 and die paddle 135, the bond pads 113 of the first semiconductor die 110 are electrically connected to respective ones of the first surfaces 131a of the leads 130 through the use of the first conductive connectors 151 (Figure 2B). Thereafter, the first surface 121a of the second semiconductor die 120 is bonded to the second surface 111b of the first semiconductor die 110 by another layer of the die attach material 160 (Figure 2C).

[0023] Subsequent to the attachment of the second semiconductor die 120 to the first semiconductor die 110, the bond pads 123 of the second semiconductor die 120 are electrically connected to respective ones of the second surfaces 131b of the leads 130 through the use of the second conductive connectors 153 in the above-described manner (Figure 2D). Thereafter, the encapsulant is applied to the first and second semiconductor dies 110, 120, the leads 130 and the first and second conductive connectors 151, 153 to encapsulate the same and form the encapsulating portion 180 (Figure 2E). As indicated above, the encapsulating portion 180 protects the first and second semiconductor dies 110, 120, the leads 130, and the first and second conductive connectors 151, 153 from the external environment.

[0024] It is contemplated that the second semiconductor die 120 may be bonded to the first semiconductor die 110 via a layer of the die attach material 160, with the first semiconductor die 110 thereafter being bonded to the leads 130 in the above-described manner. It is further contemplated that the bonding order of the first and second

conductive connectors 151, 153 used to facilitate the electrical connection of the first and second semiconductor dies 110, 120, respectively, to the leads 130 can be changed or reversed from that described above if warranted by the circumstance.

[0025] This disclosure provides exemplary embodiments of the present invention. The scope of the present invention is not limited by these exemplary embodiments. Numerous variations, whether explicitly provided for by the specification or implied by the specification, such as variations in structure, dimension, type of material or manufacturing process may be implemented by one of skill in the art in view of this disclosure.

WHAT IS CLAIMED IS:

1. A semiconductor package comprising:

a plurality of leads, each of the leads defining:

a first surface;

a second surface disposed in opposed relation to the first surface; and

a third surface disposed in opposed relation to the second surface, the first surface being oriented between the second and third surfaces;

a first semiconductor die defining opposed first and second surfaces and including a plurality of bond pads disposed on the first surface thereof, the first surface of the first semiconductor die being attached to the second surface of each of the leads;

a second semiconductor die defining opposed first and second surfaces and including a plurality of bond pads disposed on the second surface thereof, the first surface of the second semiconductor die being attached to the second surface of the first semiconductor die;

a plurality of conductive connectors electrically connecting the bond pads of the first and second semiconductor dies to respective ones of the leads; and

an encapsulating portion applied to and at least partially encapsulating the leads, the first and second semiconductor dies, and the conductive connectors.

2. The semiconductor package of Claim 1 wherein the conductive connectors comprise conductive wires.

3. The semiconductor package of Claim 2 wherein:

the conductive wires comprise first and second conductive wires;

the bond pads of the first semiconductor die are electrically connected to respective ones of the first

surfaces of the leads by respective ones of the first conductive wires; and

the bond pads of the second semiconductor die are electrically connected to respective ones of the second surfaces of the leads by respective ones of the second conductive wires.

4. The semiconductor package of Claim 1 further comprising:

a die paddle defining opposed top and bottom surfaces, the leads being disposed about the die paddle;

the first surface of the first semiconductor die further being attached to the top surface of the die paddle.

5. The semiconductor package of Claim 4 wherein:

the first surface of the first semiconductor die is attached to the second surface of each of the leads and to the top surface of the die paddle by a first bonding means; and

the first surface of the second semiconductor die is attached to the second surface of the first semiconductor die by a second bonding means.

6. The semiconductor package of Claim 4 wherein:

the die paddle is formed to have a die paddle thickness;

each of the leads is formed to have a lead thickness between the second and third surfaces thereof; and

the die paddle thickness is substantially equal to the lead thickness.

7. The semiconductor package of Claim 4 wherein the encapsulating portion is applied to the die paddle such that the bottom surface of the die paddle is exposed within the encapsulating portion.

8. The semiconductor package of Claim 7 wherein the

encapsulating portion is applied to the leads such that the third surface of each of the leads is exposed within the encapsulating portion.

9. The semiconductor package of Claim 1 wherein the encapsulating portion is applied to the leads such that the third surface of each of the leads is exposed within the encapsulating portion.

10. The semiconductor package of Claim 1 wherein the first semiconductor die and the leads are oriented relative to each other such that each of the bond pads of the first semiconductor die is located between a respective pair of the leads so that the bond pads of the first semiconductor die do not contact the second surface of any one of the leads.

11. The semiconductor package of Claim 10 wherein:

the first semiconductor die defines a peripheral edge; and

the conductive connectors electrically connecting the bond pads of the first semiconductor die to the leads are oriented inwardly relative to the peripheral edge of the first semiconductor die.

12. A method of fabricating a semiconductor package, comprising the steps of:

a) providing a plurality of leads, each of the leads having a first surface, a second surface disposed in opposed relation to the first surface, and a third surface disposed in opposed relation to the second surface, the first surface being oriented between the second and third surfaces;

b) attaching a first surface of a first semiconductor die to the first surface of each of the leads;

c) attaching a first surface of a second semiconductor die to a second surface of the first semiconductor die;

d) electrically connecting bond pads disposed on the first surface of the first semiconductor die and a second surface of the second semiconductor die to respective ones of the leads; and

e) applying an encapsulant to the first and second semiconductor dies and the leads to form an encapsulating portion which at least partially encapsulates the first and second semiconductor dies and the leads.

13. The method of Claim 12 wherein step (d) comprises:

1) electrically connecting the bond pads of the first semiconductor die to respective ones of the first surfaces of the leads by respective ones of first conductive wires; and

2) electrically connecting the bond pads of the second semiconductor die to respective ones of the second surfaces of the leads by respective ones of second conductive wires.

14. The method of Claim 12 wherein:

step (a) further comprises providing a die paddle defining opposed top and bottom surfaces, the leads being disposed about the die paddle; and

step (b) further comprises attaching the first surface of the first semiconductor die to the top surface of the die paddle.

15. The method of Claim 14 wherein:

step (b) comprises bonding the first surface of the first semiconductor die to the second surface of each of the leads and the top surface of the die paddle; and

step (c) comprises bonding the first surface of the second semiconductor die to the second surface of the first semiconductor die.

16. The method of Claim 14 wherein step (e) comprises

applying the encapsulant to the leads such that the third surface of each of the leads is exposed within the encapsulating portion.

17. The method of Claim 16 wherein step (e) comprises applying the encapsulant to the die paddle such that the bottom surface of the die paddle is exposed within the encapsulating portion.

18. The method of Claim 12 wherein step (e) comprises applying the encapsulant to the leads such that the third surface of each of the leads is exposed within the encapsulating portion.

SEMICONDUCTOR PACKAGE WITH STACKED DIES

ABSTRACT OF THE DISCLOSURE

[0026] A semiconductor package comprising a plurality of leads. Each of the leads defines opposed first and second surfaces, and a third surface which is also disposed in opposed relation to the second surface. The first surface is oriented between the second and third surfaces. The semiconductor package further comprises first and second semiconductor dies which each define opposed first and second surfaces. Disposed on the first surface of the first semiconductor die are a plurality of bond pads, with bond pads also being disposed on the second surface of the semiconductor die. The first surface of the first semiconductor die is attached to the second surface of each of the leads, with the first surface of the second semiconductor die being attached to the second surface of the first semiconductor die. A plurality of conductive connectors or wires electrically connect the bond pads of the first and second semiconductor dies to respective ones of the leads. An encapsulating portion is applied to and at least partially encapsulates the leads, the first and second semiconductor dies, and the conductive connectors.

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Draft 1

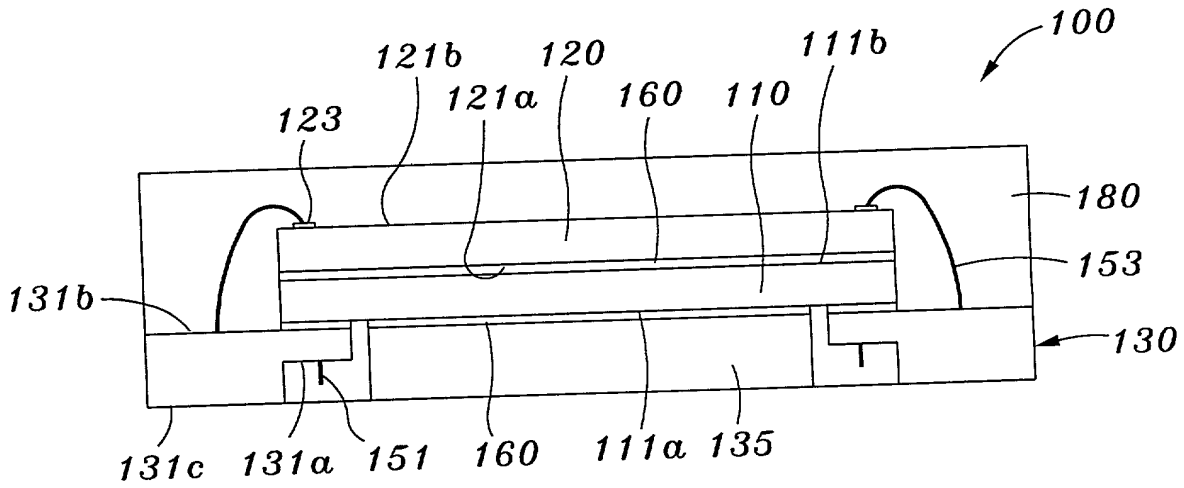

100
121b
120
111b
121a
160
110
123
180
153
131b
130
131c
131a
151
160
111a
135

FIG. 1

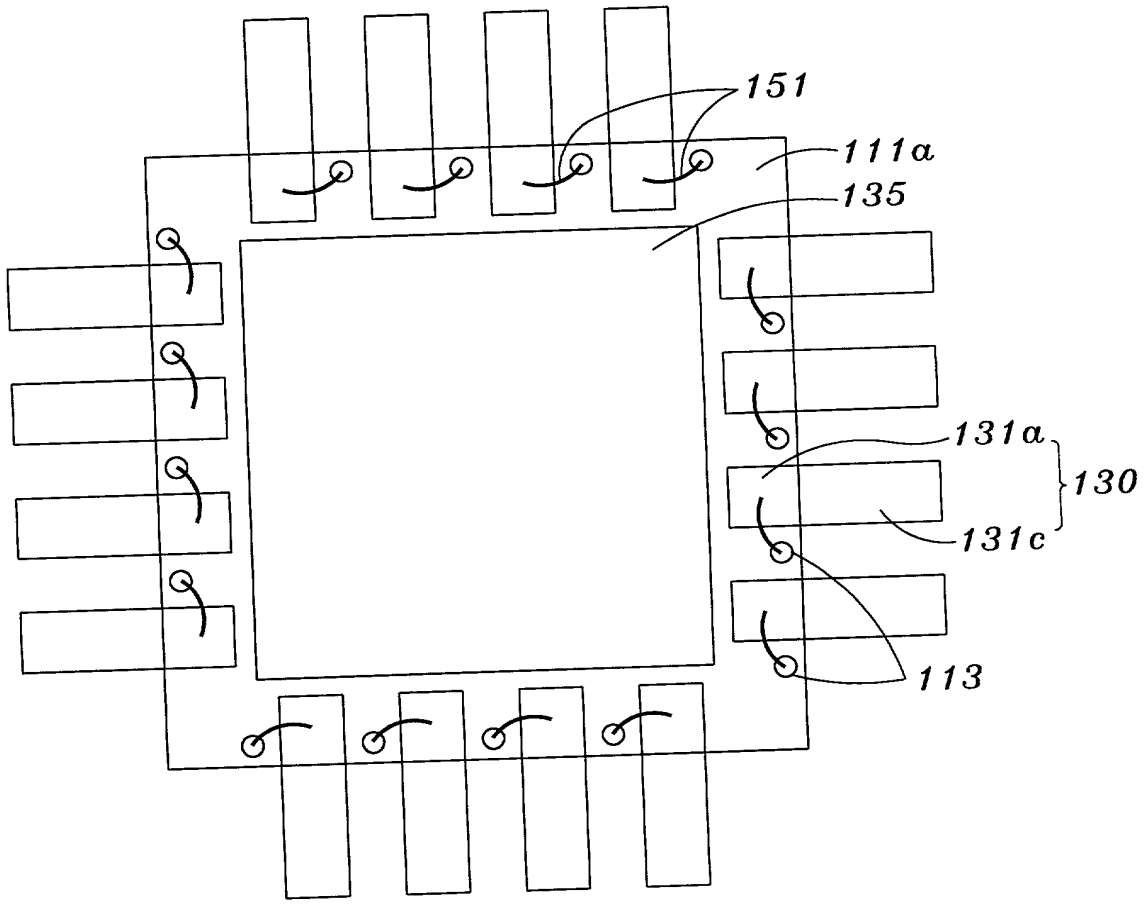

151
111a
135
131a
130
131c
113

FIG. 1A

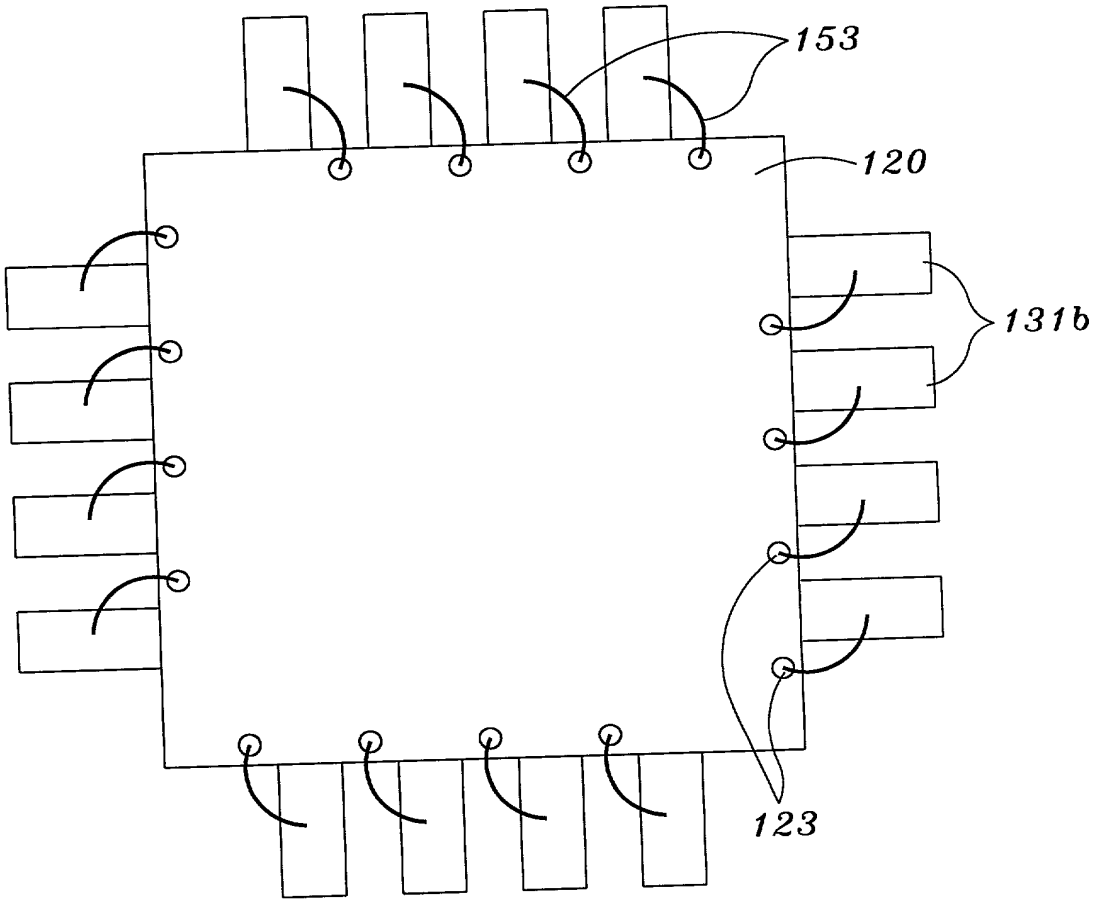


FIG. IB

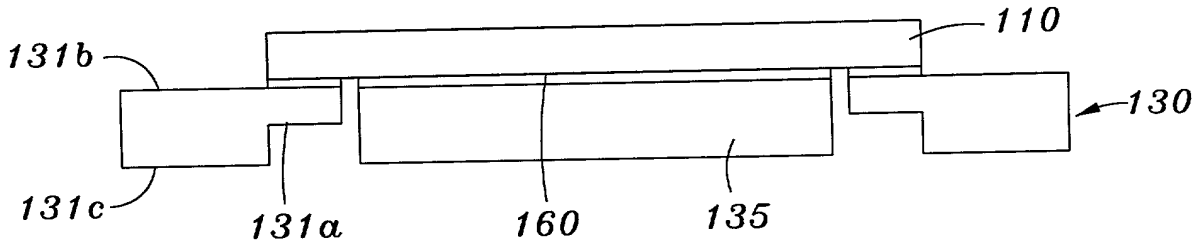


FIG. 2A

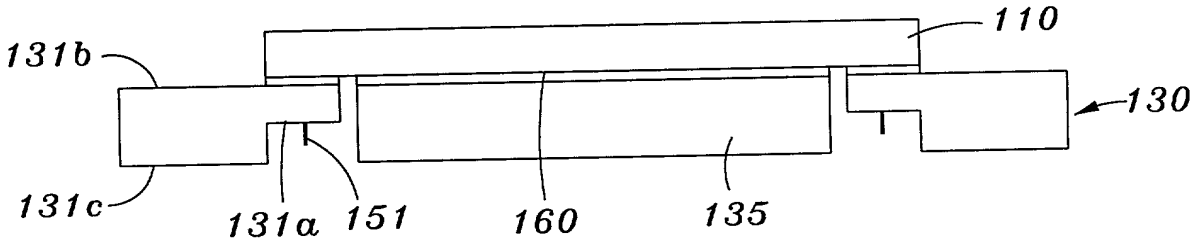


FIG. 2B

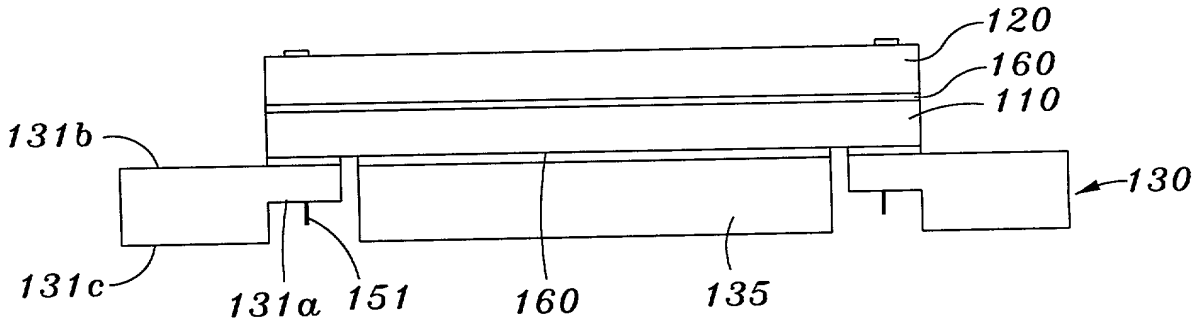


FIG. 2C

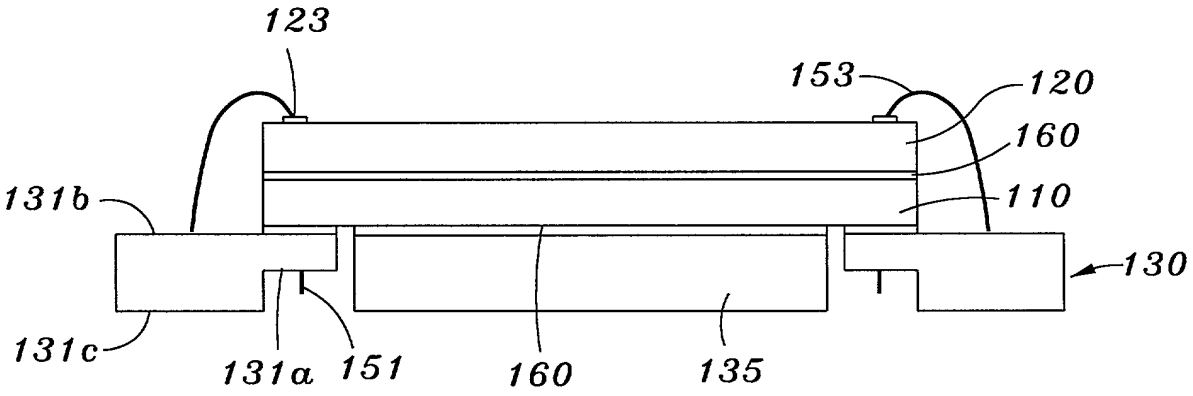
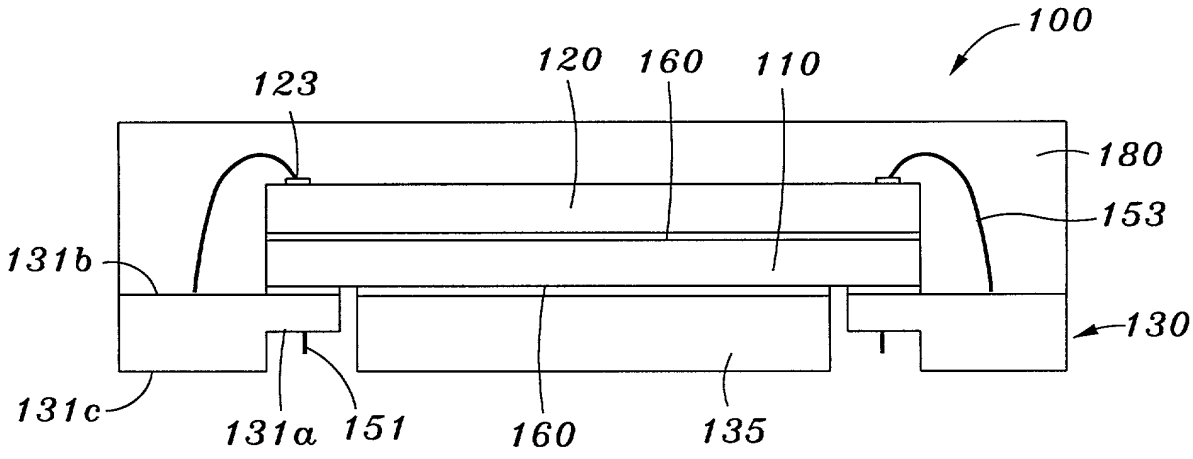

123
153
120
160
110
131b
130
131c
131a
151
160
135

FIG. 2D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120
160
110
123
180
153
131b
130
131c
131a
151
160
135

FIG. 2E

PTO/SB/01 (12-97) †

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DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION (37 CFR 1.63)

☒ Declaration Submitted with Initial Filing OR ☐ Declaration Submitted after Initial Filing (surcharge (37 CFR 1.16(e) required)

Attorney Docket Number	AMKOR-017A
First Named Inventor	Jong Sik Paek
COMPLETE IF KNOWN	
Application Number	Unknown
Filing Date	Herewith
Group Art Unit	Unknown
Examiner Name	Unknown

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

SEMICONDUCTOR PACKAGE WITH STACKED DIES

(Title of Invention)

the specification of which

☒ is attached hereto

OR

☐ was filed on (MM/DD/YYYY) _____ as United States Application Number or PCT International Application Number _____ and was amended on (MM/DD/YYYY) _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached YES	Certified Copy Attached NO
2001-02163	Korea	01/15/2001	☐	☐	☐

☐ Additional foreign application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

I hereby claim the benefit under 35 U.S.C. 119(e) of any United States provisional application(s) listed below.

Application Number(s)	Filing Date (MM/DD/YYYY)	☐ Additional provisional application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

† SEND TO: Assistant Commissioner for Patents, Washington, D.C. 20231

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DECLARATION — Utility or Design Patent Application

I hereby claim the benefit under 35 U.S.C. 120 of any United States application(s), or 365(c) of any PCT international application designating the United States of America, listed below and insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of 35 U.S.C. 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

U.S. Parent Application or PCT Parent Number	Parent Filing Date (MM/DD/YYYY)	Parent Patent Number (if applicable)

☐ Additional U.S. or PCT international application numbers are listed on a supplemental priority data sheet PTO/SB/02 attached hereto.

As a named inventor, I hereby appoint the following registered practitioner(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith: ☒ Customer Number 007663 OR ☐ Registered practitioner(s) name/registration number listed below

Place Customer No. Bar Code Label Here

Name	Registration Number	Name	Registration Number

☐ Additional registered practitioner(s) named on supplemental Registered Practitioner Information sheet PTO/SB/02C attached hereto.

Direct all correspondence to: ☒ Customer Number or Bar Code Label 007663 OR ☐ Correspondence Address Below

Name							
Address							
Address							
City			State		ZIP		
Country		Telephone			Fax		

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Name of Sole or First Inventor:	☐ A petition has been filed for this unsigned inventor						
Given Name (first and middle (if any))			Family Name or Surname				
Jong Sik			Park				
Inventor's Signature	[signature]					Date	01/08/2002
Residence: City	Kwangju-shi	State		Country	Rep of Korea	Citizenship	Rep. of Korea
Post Office Address	101-203 Daeju Apt. Unam-dong, Puk-gu, Kwangju-shi Rep. of Korea						
Post Office Address							
City	Kwangju-shi	State		ZIP		Country	Rep. of Korea

☐ Additional inventors are being named on the ___ supplemental Additional Inventor(s) sheet(s) PTO/SB/02A attached hereto.